In the claims:

Following is a complete set of claims as amended with this Response.

1-10. (Canceled)

11. (Currently Amended) A memory map for interleaved memory comprising:

a first channel having a data channel width and having a first sequence of pairs of consecutive data blocks, each data block having the same number of bits as the width of the data channel; and

a second channel having the same data channel width as the first channel and having a second sequence of pairs of consecutive data blocks, the pairs of the first sequence having the same number of bits as the pairs in the second sequence and alternating in sequential order with the pairs of the second sequence.

12. (Original) The memory map of Claim 11, wherein the first sequence of pairs consists of odd pairs and the second sequence consists of even pairs.

13. (Original) The memory map of Claim 11, wherein the data blocks are numbered sequentially, wherein the first sequence of pairs comprises a pair of blocks 0,1 and a pair of blocks 4 and 5, and wherein the second sequence of pairs comprises a pair of blocks 2 and 3 and a pair of blocks 6 and 7.

14. (Original) The memory map of Claim 11, wherein the first and second sequences of pairs have a transition interval and wherein after each occurrence of the interval the first and second sequences reverse order.

15. (Original) The memory map of Claim 14, wherein the first sequence of pairs consists of odd pairs before the first transition point and the second sequence consists of even pairs, and wherein the first sequence consists of even pairs after the first transition interval and before a second transition interval, and wherein the second sequence consists of odd pairs after the first transition interval and before the second transition interval.

16. (Original) The memory map of Claim 14, wherein the first and second sequences are chosen to optimize memory access speed by a selected controller.

17. (Original) The memory map of Claim 16, wherein the controller is a graphics processor.

18-29. (Canceled)

30. (Currently Amended) A computer system comprising:

a graphics controller;

a dual channel memory, each channel having a data channel width corresponding to a number of bits;

a central processing unit; and

a memory controller coupled by a bus to the CPU, the dual channel memory and the graphics controller, the memory controller having a memory map to the first channel of the dual channel memory having a first sequence of pairs of consecutive data blocks, and memory map to the second channel of the dual channel memory having a second sequence of pairs of consecutive data blocks, the pairs of the first sequence alternating in sequential order with the pairs of the second sequence, each data block having the same number of bits as the data channel width.

31. (Original) The system of Claim 30, wherein the first and second sequences of pairs have a transition interval and wherein after each occurrence of the interval the first and second sequences reverse order.

32. (Original) The system of Claim 30, wherein the first sequence of pairs consists of odd pairs before the first transition point and the second sequence consists of even pairs, and wherein the first sequence consists of even pairs after the first transition interval and before a second transition interval, and wherein the second sequence consists of odd pairs after the first transition interval and before the second transition interval.

33. (Previously Presented) The system of Claim 30, wherein the memory controller:

maps a first pair of data blocks to a first channel of a dual channel memory;

maps a second pair of data blocks to a second channel of the dual channel memory;

maps a third pair of data blocks to the first channel of the dual channel memory;

maps a fourth pair of data blocks to the second channel of the dual channel memory;

maps a fifth pair of data blocks to the second channel of the dual channel memory; and

maps a sixth pair of data blocks to the first channel of the dual channel memory.

34. (Previously Presented) The system of Claim 33, wherein the data blocks each comprise a quadword.

35. (Previously Presented) The system of Claim 34, wherein each pair of data blocks consists of two sequential quadwords.

36. (Previously Presented) The system of Claim 35, wherein the first, second, third and fourth pairs combined contain of 64 bytes.

37. (Previously Presented) The system of Claim 30, wherein the memory controller detects devices coupled to a memory controller, selects a primary device from among the detected devices for memory access, and selects a system memory memory map to optimize system memory operation with the selected device.

38. (Previously Presented) The system of Claim 37, wherein detecting devices comprises detecting the CPU and the graphics controller.

39. (Previously Presented) The system of Claim 37, wherein selecting a primary device comprises determining a memory configuration for the graphics controller.

40. (Previously Presented) The system of Claim 37, wherein selecting a primary device comprises selecting the CPU if the graphics controller includes internal memory and selecting the graphics controller if the graphics controller uses system memory.

41. (Previously Presented) The system of Claim 37, wherein selecting a memory map comprises selecting a system memory map to optimize graphics memory access if the graphics controller is selected.

42. (Previously Presented) The memory map of Claim 11, wherein the adjacent data blocks of the first pair have adjacent address values.

43. (Previously Presented) The memory map of Claim 11, wherein the data blocks each consist of a fixed number of bytes and the first block of the first pair is spaced apart from the first block of the second block by eight times the fixed number.

44. (Previously Presented) The memory map of Claim 11, wherein the interleaved memory is a double data rate memory device.

45. (Previously Presented) The memory map of Claim 11, wherein the data blocks are accessible to a graphics controller

46. (Previously Presented) The memory map of Claim 11, wherein data is written into the memory from a graphics controller.

47. (Previously Presented) The memory map of Claim 11, wherein the first and second sequence of pairs are simultaneously accessible.